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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/806,224	06/11/2001	Hartmut Grutzediek	1477.011	4906

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EXAMINER
FOURSON III, GEORGE R

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/806,224	GRUTZEDIEK ET AL.	
	Examiner	Art Unit	
	George Fourson	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27 and 29-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27 and 29-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/2/05 has been entered.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-27 and 29-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakurai et al alone or in combination with Nemoto.

Sakurai et al. teaches a method of forming integrated circuit devices such as transistors, diodes and logic gates which includes providing mask 22 onto semiconductor substrate 21 (Page 2, lines 26-30, and Fig. 2), then forming window 23 delimited by peripheral edge (Page 2, lines 31-38, Fig. 3), then performing ion implantation into semiconductor substrate 21 using mask 22 to form n-doped trough 24 with fringe area of trough 24 extending up to semiconductor substrate 21 and with energy that assures n-doped inner area remains on surface of semiconductor substrate 21 (Page 3, lines 1-12, and Fig. 4), and forming additional n-doped areas 27 and 28 in p-doped inner area and in the fringe area of n-doped trough (Page, 3, lines 18-29).

Official notice that formation of an external base layer adjacent to the base layer having an impurity concentration that is higher than that of the base layer was known prior to applicant's invention was taken in the office action mailed 8/14/02 and also disclosed by Nemoto.

It would have been within the scope to one ordinary skill in the art to combine either the known process or that of Nemoto with that of Sakurai et al. because it would enable the formation of a bipolar transistor with p-doped or n-doped area having heavier doping than n-doped or p-doped inner area to be performed.

The choice of particular doping levels for the regions/areas formed would have been a matter of routine optimization to achieve the desired device densities on the finished wafer and the desired device characteristics of the device. (See MPEP 2144.05).

The recited method of formation of additional devices would have been within the scope of one ordinarily skill in the art in view of the disclosure of formation of I^2L (page 14, lines 14-15), the particular steps recited being conventional at the time of applicant's invention and/or design choices.

With respect to claims 29-30, one of ordinary skilled in the art would have been lead to the recited implant energy and doping level through routine experimentation to achieve desired device dimensions and device density on the finished wafer and, therefore, desired device characteristics because device dimension and doping levels of device elements were known to affect device performance at the time of applicant's invention. (See MPEP 2 144.05).

At page 2, lines 20-25 Sakurai states that the method was proposed in Japanese Patent application 50-364. In view of the translation of Japan '364 provided the additional implantation to obtain particular disclosed advantages, namely improved performance and preventing turnover during certain operation conditions. Therefore it would have been obvious to one of ordinary skill in the art to omit the implantation step with the expectation that the disclosed comcomitant advantages of the step would not be obtained and with a reasonable expectation of success that the method would produce a working device although one that may exhibit turnover under certain conditions.

George Fourson
Primary Examiner